REMARKS

Reconsideration is respectfully requested. Claims 8-22 were present in the application. Claims 8, 11, 13, 14, 17 and 19 are amended herein. Claims 9, 12, 15, 18 and 20-22 are canceled. Claims 10 and 16 have been allowed.

Claims 13 and 19 were indicated as allowable if rewritten to independent form, including the limitations of the base claim and any intervening claim. These claims have been so rewritten and are accordingly submitted to be allowable.

Claims 20-22 were rejected under 35 U.S.C. §101. Applicant cancels the claims herein to further the prosecution of the application, with reservation of the right to file any continuation applications directed to those claims.

Claims 8, 9, 11, 12, 14, 15, 17, 18, 20 and 21 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Mustafa et al (U.S. 6,678,831) in view of Chou et al (U.S. 5,832,283). Applicant respectfully traverses. As noted above, claims 9, 12, 15, 18, 20 and 21 have been canceled, so their rejection no longer applies.

With regard to the remaining claims, applicant respectfully traverses.

Mustafa fails, as admitted by the Examiner, to teach switching to a first and second power mode based on whether or not any timer-expiration-waiting events are scheduled to

execute. The Examiner indicates that Chou explicitly teaches entering a standby mode when timer-expiration-waiting events are scheduled to execute.

However, Chou's "standby mode" is only one power saving operation mode in the Chou system and whenever the system enters the standby mode it sets the hardware timer to return back to the normal mode at the time of its expiration. Chow s timer-expiration-waiting event is always present when entering the standby mode in the Chou system. Therefore, the presence of the timer-expiration-waiting event would never be a condition for selectively entering two different power saving operation modes in Mustafa.

Moreover, neither Mustafa nor Chou teaches the "first power saving operation mode allowing periodically occurring timer interrupts to be accepted" and "timer-expiration-waiting event, for which periodically occurring timer interrupts are used to judge timer-expiration" as recited in Applicant's claims. The periodically occurring timer interrupts in a power saving operation mode could cause the problem mentioned in Applicant's specification at page 14, lines 2-9, which reads:

> The timer interrupt operation is disabled in this way because, if the timer interrupt remained activated when there is no timer-expiration waiting event, the CPU would return from the power saving state to the normal execution state each time a timer

> interrupt is received and therefore the effect of power saving would be lost. Disabling the timer interrupt also stops the periodic processing operation of the interval handler 27 (FIG. 1).

On the other hand, the interrupt of timer (105) in Chou is a "one-shot" type timer interrupt which occurs once after the system entered the standby mode, when the timer expires (Column 12, lines 6-12). This means that there is no concern in Chou about the problem mentioned in the applicant's specification.

Therefore, there is no suggestion or motivation found in the references for combining Chou with Mustafa, and claims 8, 11, 14 and 17 are submitted to be allowable over Mustafa et al in view of Chou et al.

In light of the above noted amendments and remarks, this application is believed in condition for allowance and notice thereof is respectfully solicited. The Examiner is asked to contact applicant's attorney at 503-224-0115 if there are any questions.

Respectfully submitted,

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